Copper damascene method for ultra large scale integration circuits

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Abstract

The present invention relates to a manufacturing method which applies the copper-palladium alloy damascene technology to the fabrication of ultra large scale integration (ULSI) circuits. First, a TaN barrier is formed on an oxide layer which is known as inter metal dielectric (IMD) layer. Then, a copper-palladium seed is formed on the TaN barrier, and a copper-palladium gap-fill electroplating layer is formed on the dielectric oxide layer. Next, a copper-palladium annealing process is carried out. The copper-palladium gap-fill electroplating layer is able to depress the oxidization in the thermal process due to the existence of the palladium, thereby providing a higher oxidization output schedule in comparison with the conventional copper gap-fill electroplating layer. Then, the copper-palladium electroplating surface is planarized by means of a chemical mechanical polishing (CMP) process. Third, the CoWP cap is selectively deposited on the copper-palladium electroplating layer, wherein the palladium is a catalyst or accelerator in the self oxidation reduction step of the electrochemistry reaction. The self-alignment process of CoWP will decrease the capacitance of the IMD, and eliminate the peeling issues between the Si3N4 capped barrier layer and the copper-palladium dielectric layer. Furthermore, because of the low resistance of the CoWP, a step of etching conductive holes is not required, and thus there is nor short circuit problem caused by sputtering the copper. Fourth, a second IMD is formed on the first IMD. Finally, the steps of the above method are repeated to continue the deposition step, thereby completing the whole manufacturing process of the device.